
# STMP157-BASE-SOM

# User Manual

Rev.1.0 November 2023

olimex.com

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# What is STMP157-BASE-SOM

STMP157-BASE-SOM-EXT is system on module development board with STM32MP157DAA1 Dual Core Cortex A7 running @800Mhz + Cortex-M4 co-processor running at 209Mhz.

STM32MP157DAA1 targets industrial application and have plenty of features:

- Core
    - 32-bit dual-core Arm® Cortex®-A7
        - L1 32-Kbyte I / 32-Kbyte D for each core
        - 256-Kbyte unified level 2 cache
        - Arm® NEON™ and Arm® TrustZone®
    - 32-bit Arm® Cortex®-M4 with FPU/MPU
        - Up to 209 MHz (Up to 703 CoreMark®)
- Memories
    - External DDR memory up to 1 Gbyte
        - up to LPDDR2/LPDDR3-1066 16/32-bit
        - up to DDR3/DDR3L-1066 16/32-bit
    - 708 Kbytes of internal SRAM: 256 Kbytes of AXI SYSRAM + 384 Kbytes of AHB SRAM + 64 Kbytes of AHB SRAM in Backup domain and 4 Kbytes of SRAM in Backup domain
    - Dual mode Quad-SPI memory interface
    - Flexible external memory controller with up to 16-bit data bus: parallel interface to connect external ICs and SLC NAND memories with up to 8-bit ECC
- Security/safety
    - TrustZone® peripherals, active tamper
    - Cortex®-M4 resources isolation
- Reset and power management
    - 1.71 V to 3.6 V I/Os supply (5 V-tolerant I/Os)
    - POR, PDR, PVD and BOR
    - On-chip LDOs (RETRAM, BKPSRAM, DSI 1.2 V, USB 1.8 V, 1.1 V)
    - Backup regulator (~0.9 V)
    - Internal temperature sensors
    - Low-power modes: Sleep, Stop and Standby
    - DDR memory retention in Standby mode
    - Controls for PMIC companion chip

- Low-power consumption
    - Total current consumption down to 2 µA (Standby mode, no RTC, no LSE, no BKPSRAM, no RETRAM)
- Clock management
    - Internal oscillators: 64 MHz HSI oscillator, 4 MHz CSI oscillator, 32 kHz LSI oscillator
    - External oscillators: 8-48 MHz HSE oscillator, 32.768 kHz LSE oscillator
    - 6 × PLLs with fractional mode
- General-purpose input/outputs
    - Up to 176 I/O ports with interrupt capability
        - Up to 8 secure I/Os
        - Up to 6 Wakeup, 3 tampers, 1 active tamper
- Interconnect matrix
    - 2 bus matrices
        - 64-bit Arm® AMBA® AXI interconnect, up to 266 MHz
        - 32-bit Arm® AMBA® AHB interconnect, up to 209 MHz
- 3 DMA controllers to unload the CPU
    - 48 physical channels in total
    - 1 × high-speed general-purpose master direct memory access controller (MDMA)
    - 2 × dual-port DMAs with FIFO and request router capabilities for optimal peripheral management
- Up to 37 communication peripherals
    - 6 × $I^2C$ FM+ (1 Mbit/s, SMBus/PMBus)
    - 4 × UART + 4 × USART (12.5 Mbit/s, ISO7816 interface, LIN, IrDA, SPI slave)
    - 6 × SPI (50 Mbit/s, including 3 with full duplex $I^2S$ audio class accuracy via internal audio PLL or external clock)
    - 4 × SAI (stereo audio: $I^2S$, PDM, SPDIF Tx)
    - SPDIF Rx with 4 inputs
    - HDMI-CEC interface
    - MDIO Slave interface
    - 3 × SDMMC up to 8-bit (SD / e•MMC™/ SDIO)
    - 2 × CAN controllers supporting CAN FD protocol, out of which one supports time-triggered CAN (TTCAN)
    - 2 × USB 2.0 high-speed Host+ 1 × USB 2.0 full-speed OTG simultaneously
        - or 1 × USB 2.0 high-speed Host+ 1 × USB 2.0 high-speed OTG simultaneously
    - 10/100M or Gigabit Ethernet GMAC
        - IEEE 1588v2 hardware, MII/RMII/GMII/RGMII
    - 8- to 14-bit camera interface up to 140 Mbyte/s
- 6 analog peripherals

        - 2 × ADCs with 16-bit max. resolution (12 bits up to 4.5 Msps, 14 bits up to 4 Msps, 16 bits up to 3.6 Msps)
        - 1 × temperature sensor
        - 2 × 12-bit D/A converters (1 MHz)
        - 1 × digital filters for sigma delta modulator (DFSDM) with 8 channels/6 filters
        - Internal or external ADC/DAC reference $V_{REF+}$
- Graphics
    - 3D GPU: Vivante® - OpenGL® ES 2.0
        - Up to 26 Mtriangle/s, 133 Mpixel/s
    - LCD-TFT controller, up to 24-bit // RGB888
        - up to WXGA (1366 × 768) @60 fps or up to Full HD (1920 × 1080) @30 fps
        - Pixel clock up to 90 MHz
        - Two layers with programmable colour LUT
    - MIPI® DSI 2 data lanes up to 1 Gbps each
- Up to 29 timers and 3 watchdogs
    - 2 × 32-bit timers with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
    - 2 × 16-bit advanced motor control timers
    - 10 × 16-bit general-purpose timers (including 2 basic timers without PWM)
    - 5 × 16-bit low-power timers
    - RTC with sub-second accuracy and hardware calendar
    - 2 × 4 Cortex®-A7 system timers (secure, non-secure, virtual, hypervisor)
    - 1 × SysTick M4 timer
    - 3 × watchdogs (2 × independent and window)
- Hardware acceleration
    - HASH (MD5, SHA-1, SHA224, SHA256), HMAC
    - 2 × true random number generator (3 oscillators each)
    - 2 × CRC calculation unit
- Debug mode
    - Arm® CoreSight™ trace and debug: SWD and JTAG interfaces
    - 8-Kbyte embedded trace buffer
- 3072-bit fuses including 96-bit unique ID, up to 1184-bit available for user
- All packages are ECOPACK2 compliant

# STMP157-BASE-SOM features:

STMP157-BASE-SOM-EXT exposes all STM32MP157DAA1 GPIOs and features in very compact format. It takes care for power supply and high speed memory signals complexities.

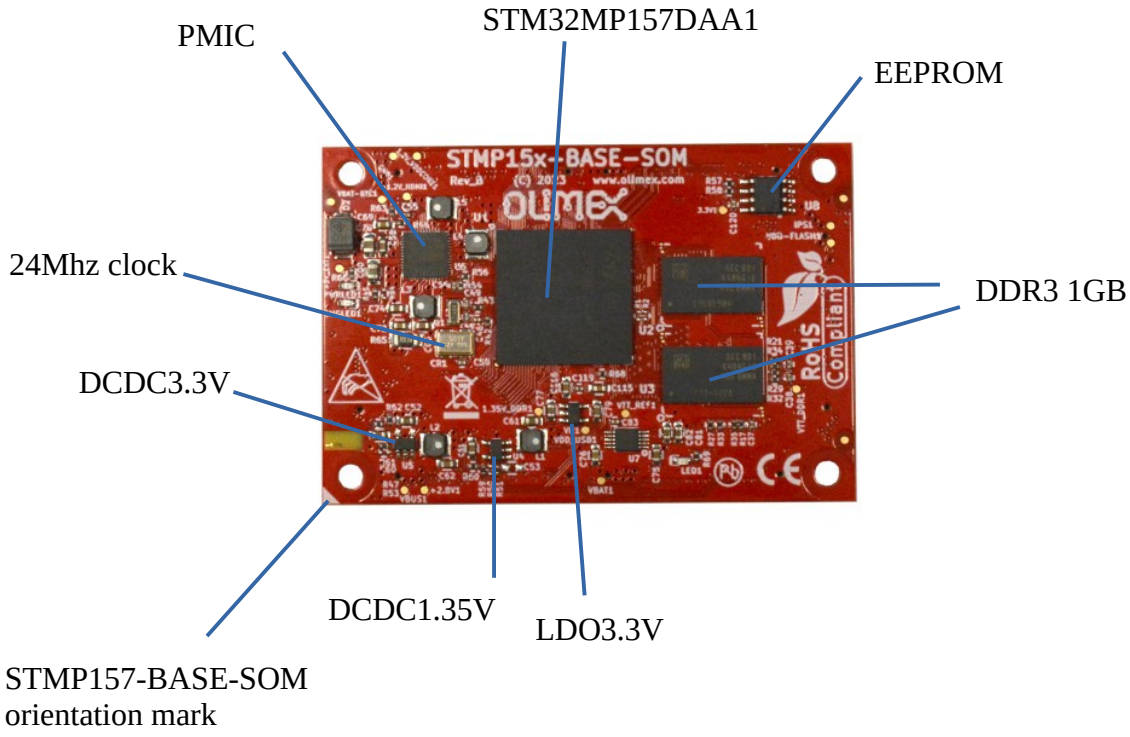
- STM32MP157DAA1 SOC Dual core Cortex-A7 + Cortex-M4 800Mhz/209Mhz
- 1GB DDR3 RAM
- AXP209 PMIC, DCDC, LDO power supply
- 24 Mhz oscillator
- Linux configuration EEPROM
- User LED
- 6 x 40 pin total 240 pin connectors with 1.27 mm/0.05" step
- Operating temperature -20+85C
- Dimensions: 72 x 48 mm (2.8x1.9")

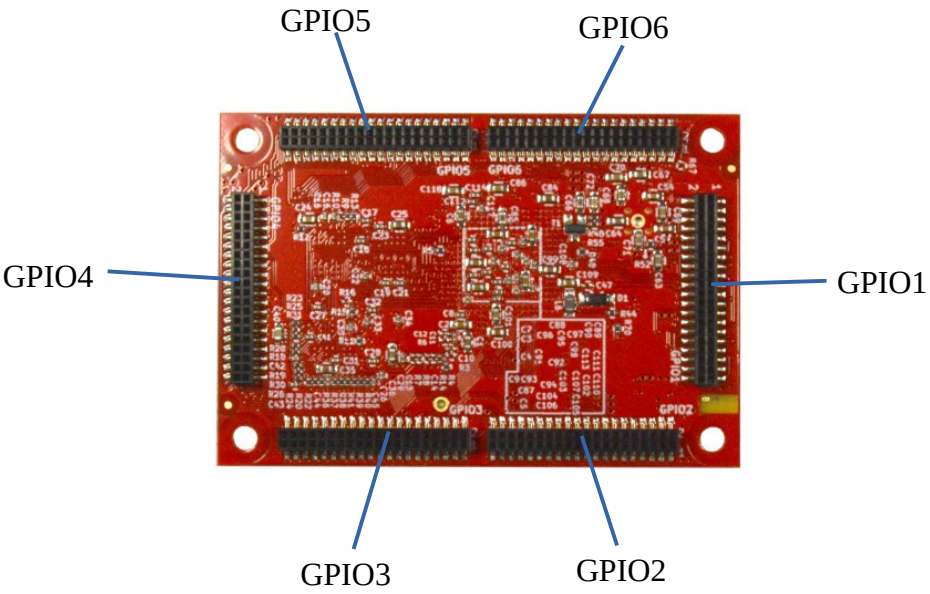
## Order codes for STMP157-BASE-SOM-EXT and accessories:

| | |
|---|---|
| STMP157-BASE-SOM-EXT | system on module with 1GB RAM, EEPROM, PMIC |
| STMP157-BASE-SOM-EVB | evaluation board for STMP157-BASE-SOM-EXT which can be used as reference design |
| MICRO-SD-16GB-CLASS10 | 16GB microSD card |
| SY1005E | power adapter 5V 2A |
| USB-SERIAL-F | serial debug cable for console log |
| CABLE-HDMI-50CM | HDMI cable |
| BATTERY-LIPO1400mAh | LiPo battery for standalone operation |
| LCD/LCD-OLinuXino-5CTS | 5 inch LCD 800x480 pixels with capacitive touch panel |
| LCD-OLinuXino-7CTS | 7 inch LCD 1024x600 pixels with capacitive touch panel |
| LCD-OLinuXino-10CTS | 10 inch LCD 1024x600 pixels with capacitive touch panel |
| UEXT modules | There are temperature, humidity, pressure, magnetic field, light sensors. Modules with LCDs, LED matrix, Relays, Bluetooth, Zigbee, WiFi, GSM, GPS, RFID, RTC, EKG, sensors and etc. |

# HARDWARE

## STMP157-BASE-SOM layout:

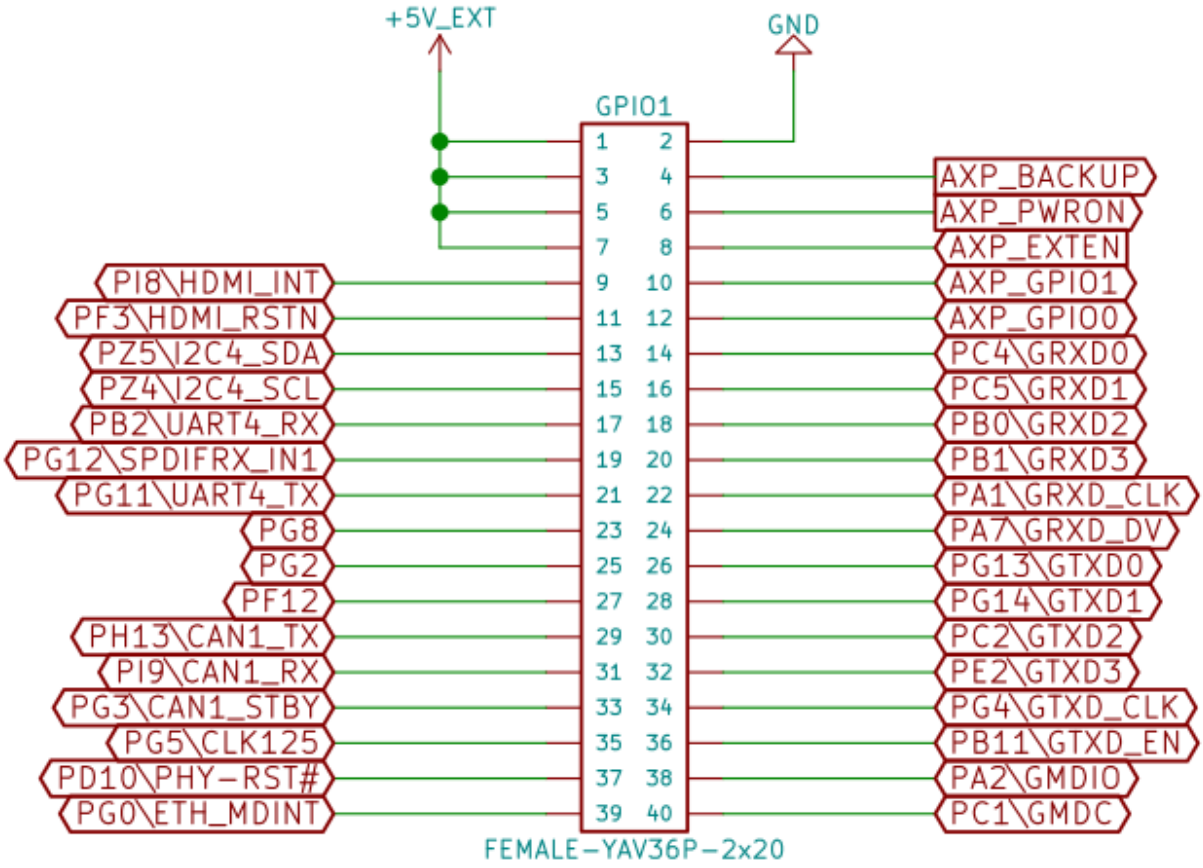


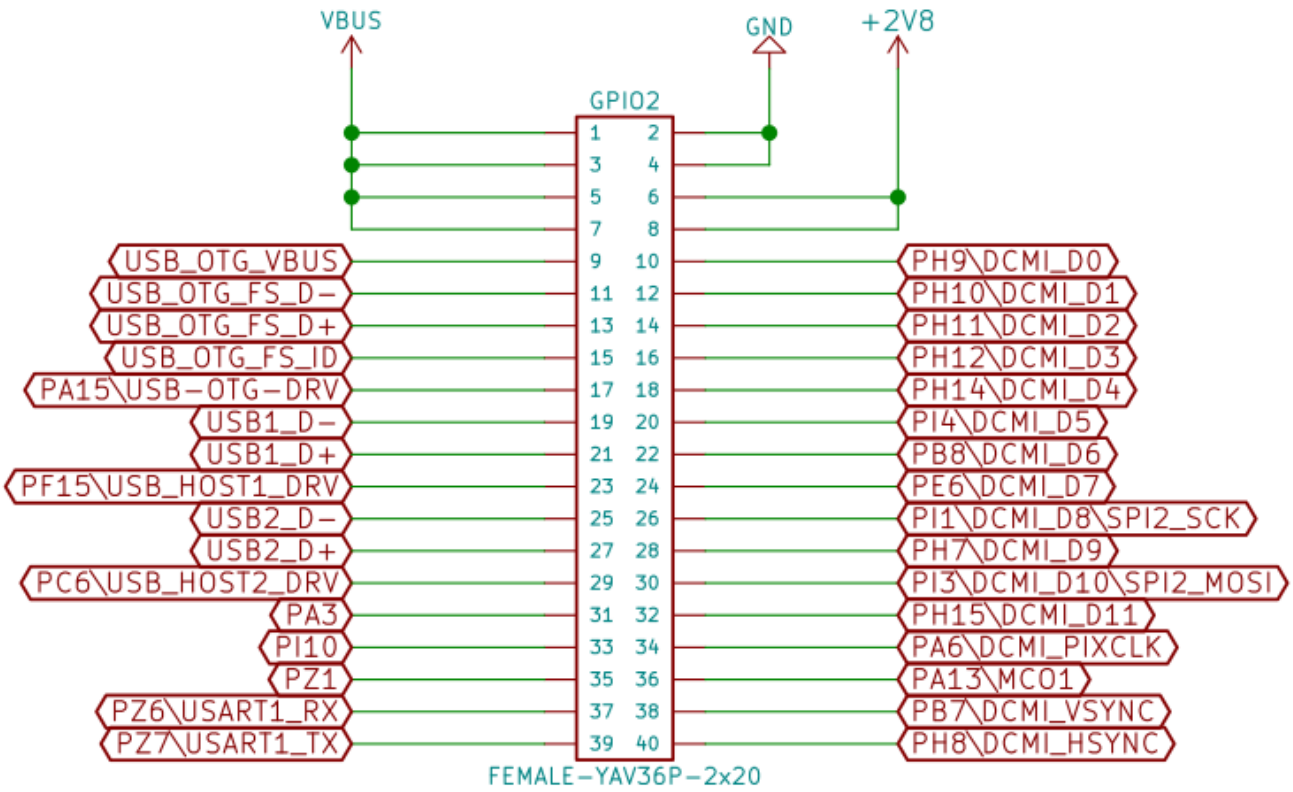

GPIO5
GPIO6
GPIO4
GPIO1
GPIO3
GPIO2

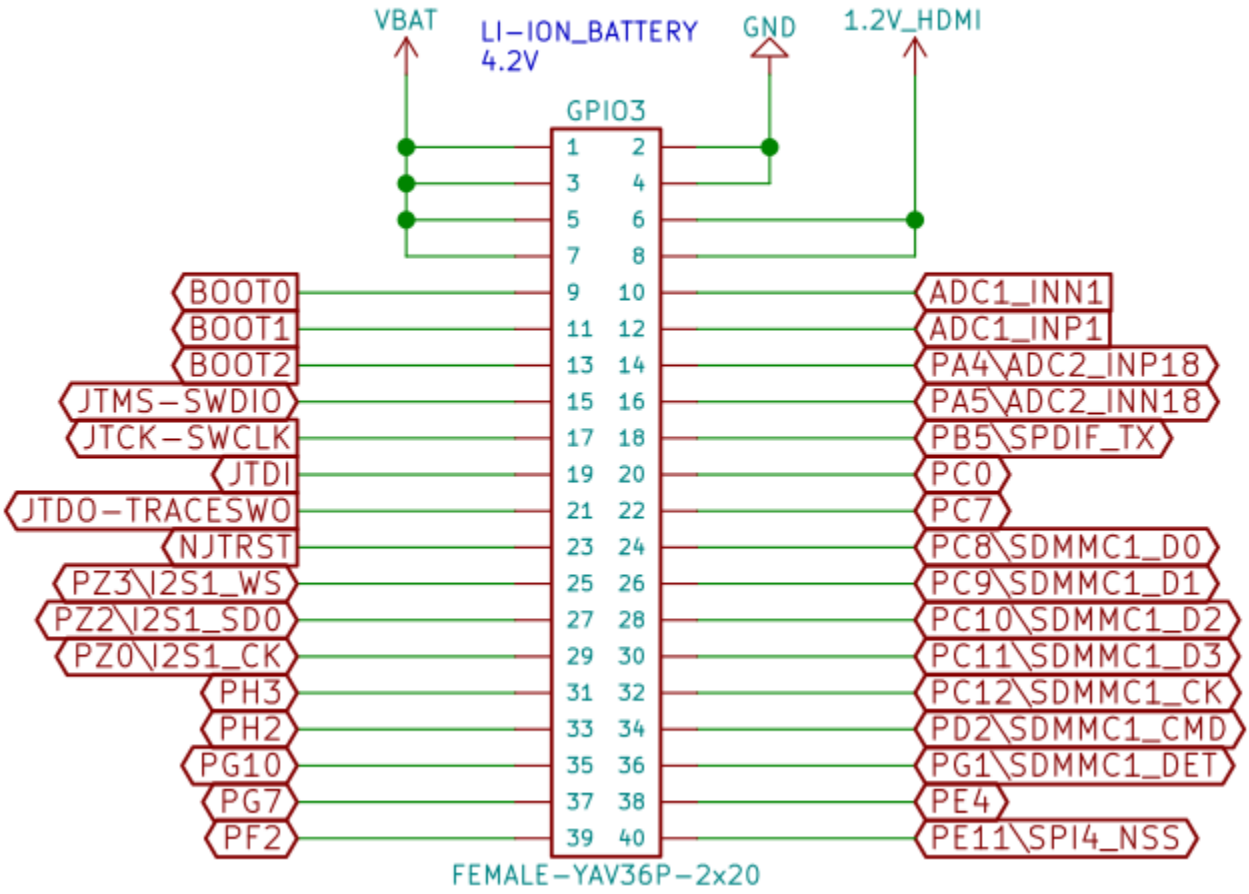
## STMP157-BASE-SOM schematics:

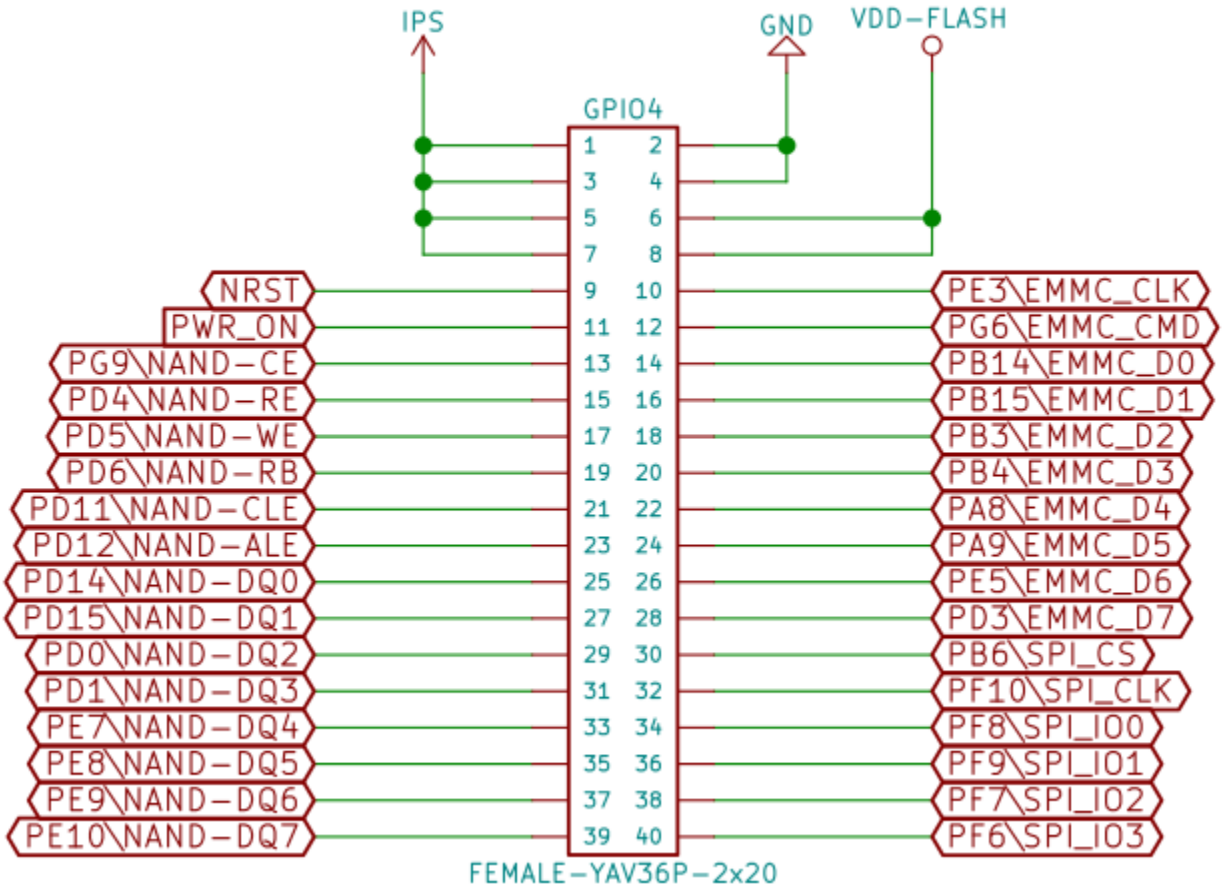
STMP157-BASE-SOM-EXT latest schematic is on Olimex web

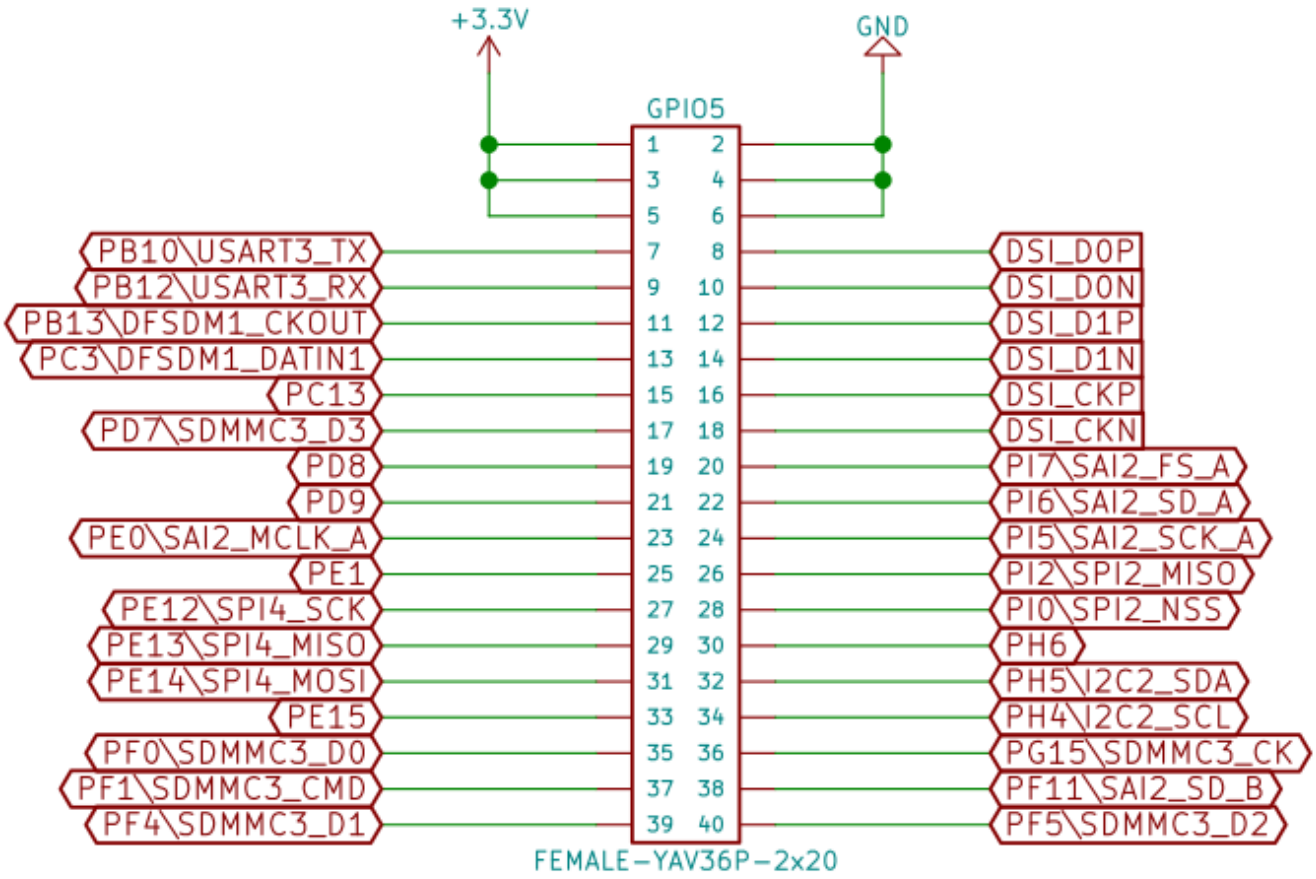
## SOM connectors:

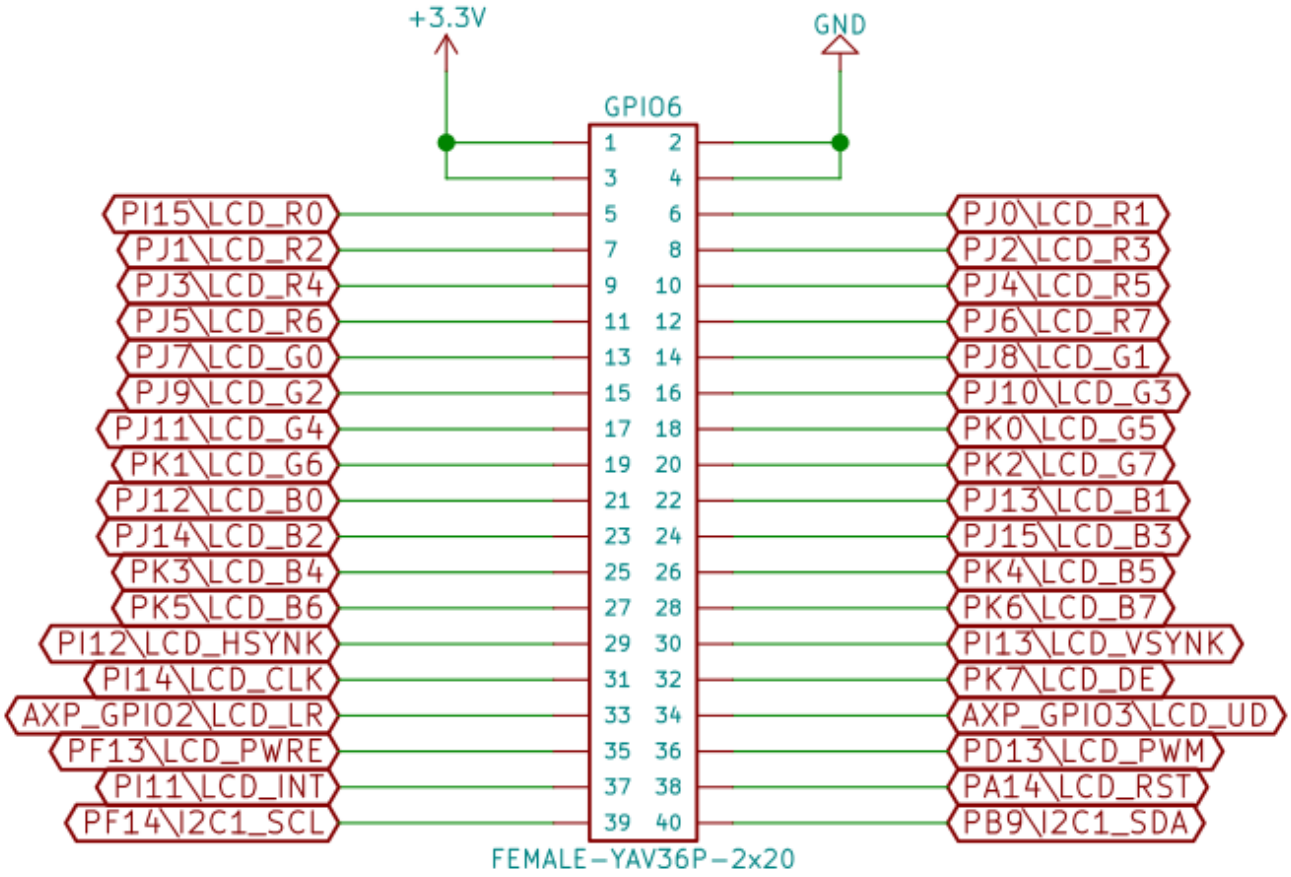



VBUS
GND
+2V8
GPIO2
1 2
3 4
5 6
7 8
USB_OTG_VBUS 9 10 PH9\DCMI_D0
USB_OTG_FS_D- 11 12 PH10\DCMI_D1
USB_OTG_FS_D+ 13 14 PH11\DCMI_D2
USB_OTG_FS_ID 15 16 PH12\DCMI_D3
PA15\USB-OTG-DRV 17 18 PH14\DCMI_D4
USB1_D- 19 20 PI4\DCMI_D5
USB1_D+ 21 22 PB8\DCMI_D6
PF15\USB_HOST1_DRV 23 24 PE6\DCMI_D7
USB2_D- 25 26 PI1\DCMI_D8\SPI2_SCK
USB2_D+ 27 28 PH7\DCMI_D9
PC6\USB_HOST2_DRV 29 30 PI3\DCMI_D10\SPI2_MOSI
PA3 31 32 PH15\DCMI_D11
PI10 33 34 PA6\DCMI_PIXCLK
PZ1 35 36 PA13\MCO1
PZ6\USART1_RX 37 38 PB7\DCMI_VSYNC
PZ7\USART1_TX 39 40 PH8\DCMI_HSYNC
FEMALE-YAV36P-2x20

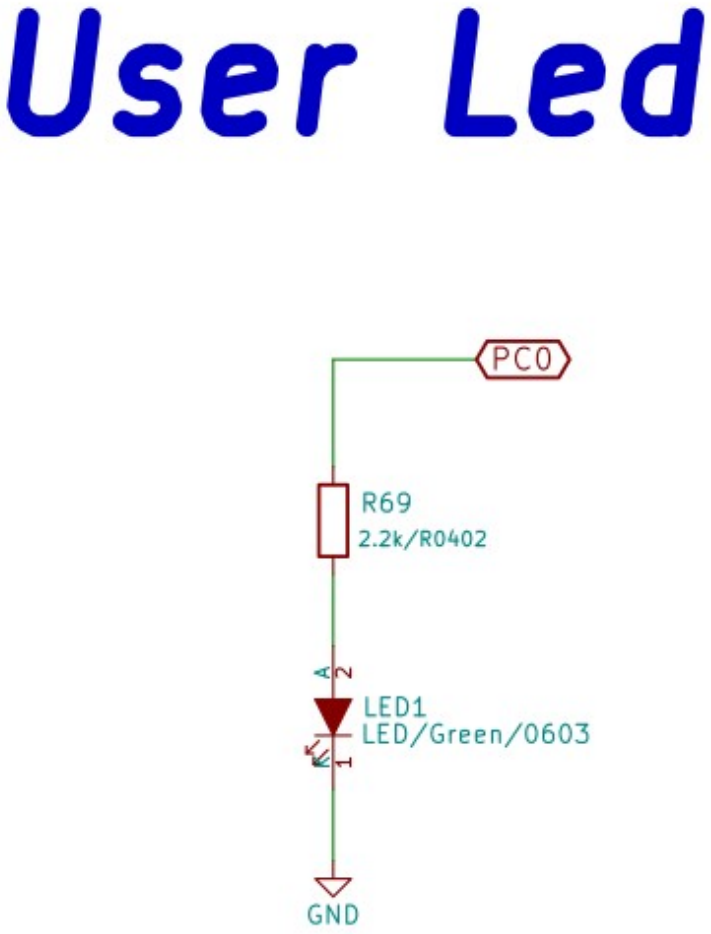

VBAT
LI-ION_BATTERY
4.2V
GND
1.2V_HDMI
GPIO3
1 2
3 4
5 6
7 8
BOOT0 9 10 ADC1_INN1
BOOT1 11 12 ADC1_INP1
BOOT2 13 14 PA4\ADC2_INP18
JTMS-SWDIO 15 16 PA5\ADC2_INN18
JTCK-SWCLK 17 18 PB5\SPDIF_TX
JTDI 19 20 PC0
JTDO-TRACESWO 21 22 PC7
NJTRST 23 24 PC8\SDMMC1_D0
PZ3\I2S1_WS 25 26 PC9\SDMMC1_D1
PZ2\I2S1_SD0 27 28 PC10\SDMMC1_D2
PZ0\I2S1_CK 29 30 PC11\SDMMC1_D3
PH3 31 32 PC12\SDMMC1_CK
PH2 33 34 PD2\SDMMC1_CMD
PG10 35 36 PG1\SDMMC1_DET
PG7 37 38 PE4
PF2 39 40 PE11\SPI4_NSS
FEMALE-YAV36P-2x20


IPS
GND
VDD-FLASH
GPIO4
1 2
3 4
5 6
7 8
NRST 9 10 PE3\EMMC_CLK
PWR_ON 11 12 PG6\EMMC_CMD
PG9\NAND-CE 13 14 PB14\EMMC_D0
PD4\NAND-RE 15 16 PB15\EMMC_D1
PD5\NAND-WE 17 18 PB3\EMMC_D2
PD6\NAND-RB 19 20 PB4\EMMC_D3
PD11\NAND-CLE 21 22 PA8\EMMC_D4
PD12\NAND-ALE 23 24 PA9\EMMC_D5
PD14\NAND-DQ0 25 26 PE5\EMMC_D6
PD15\NAND-DQ1 27 28 PD3\EMMC_D7
PD0\NAND-DQ2 29 30 PB6\SPI_CS
PD1\NAND-DQ3 31 32 PF10\SPI_CLK
PE7\NAND-DQ4 33 34 PF8\SPI_IO0
PE8\NAND-DQ5 35 36 PF9\SPI_IO1
PE9\NAND-DQ6 37 38 PF7\SPI_IO2
PE10\NAND-DQ7 39 40 PF6\SPI_IO3
FEMALE-YAV36P-2x20


+3.3V
GND
GPIO5
1 2
3 4
5 6
PB10\USART3_TX 7 8 DSI_D0P
PB12\USART3_RX 9 10 DSI_D0N
PB13\DFSDM1_CKOUT 11 12 DSI_D1P
PC3\DFSDM1_DATIN1 13 14 DSI_D1N
PC13 15 16 DSI_CKP
PD7\SDMMC3_D3 17 18 DSI_CKN
PD8 19 20 PI7\SAI2_FS_A
PD9 21 22 PI6\SAI2_SD_A
PE0\SAI2_MCLK_A 23 24 PI5\SAI2_SCK_A
PE1 25 26 PI2\SPI2_MISO
PE12\SPI4_SCK 27 28 PI0\SPI2_NSS
PE13\SPI4_MISO 29 30 PH6
PE14\SPI4_MOSI 31 32 PH5\I2C2_SDA
PE15 33 34 PH4\I2C2_SCL
PF0\SDMMC3_D0 35 36 PG15\SDMMC3_CK
PF1\SDMMC3_CMD 37 38 PF11\SAI2_SD_B
PF4\SDMMC3_D1 39 40 PF5\SDMMC3_D2
FEMALE-YAV36P-2x20


+3.3V
GND
GPIO6
1 2
3 4
PI15\LCD_R0
PJ1\LCD_R2
PJ3\LCD_R4
PJ5\LCD_R6
PJ7\LCD_G0
PJ9\LCD_G2
PJ11\LCD_G4
PK1\LCD_G6
PJ12\LCD_B0
PJ14\LCD_B2
PK3\LCD_B4
PK5\LCD_B6
PI12\LCD_HSYNK
PI14\LCD_CLK
AXP_GPIO2\LCD_LR
PF13\LCD_PWRE
PI11\LCD_INT
PF14\I2C1_SCL
5 6
7 8
9 10
11 12
13 14
15 16
17 18
19 20
21 22
23 24
25 26
27 28
29 30
31 32
33 34
35 36
37 38
39 40
PJ0\LCD_R1
PJ2\LCD_R3
PJ4\LCD_R5
PJ6\LCD_R7
PJ8\LCD_G1
PJ10\LCD_G3
PK0\LCD_G5
PK2\LCD_G7
PJ13\LCD_B1
PJ15\LCD_B3
PK4\LCD_B5
PK6\LCD_B7
PI13\LCD_VSYNK
PK7\LCD_DE
AXP_GPIO3\LCD_UD
PD13\LCD_PWM
PA14\LCD_RST
PB9\I2C1_SDA
FEMALE-YAV36P-2x20

## User LED



**Boot selection:**


| Boot Mode | Boot2 | Boot1 | Boot0 |
|---|---|---|---|
| Reserved (NoBoot) | 1 | 0 | 0 |
| NOR -> Serial NOR Flash on QUADSPI | 0 | 0 | 1 |
| NAND -> Serial NAND Flash on QUADSPI | 1 | 1 | 1 |
| NAND -> SLC NAND Flash on FMC | 0 | 1 | 1 |
| eMMC on SDMMC2 | 0 | 1 | 0 |
| SD-Card on SDMMC1 (default) | 1 | 0 | 1 |
| Forced UART/USB Boot. USB high-speed device, or USART2/3/6 and UART4/5/7/8 on default pins. | 1 | 1 | 0 |
| | 0 | 0 | 0 |

# SOFTWARE

- Recommended Olimage Linux images and changelog
- Olimage Linux guide

# Revision History

Revision 1.0 November 2023 initial